# Hu Jinhai

Scientist, Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore
Ph.D. Candidate, School of Electrical and Electronic Engineering (EEE), Nanyang Technological University (NTU), Singapore

+65 82802848 | jinhai001@e.ntu.edu.sg | github.com/HUJH511 | linkedin.com/in/jinhai-hu


## Summary of Capability

- Focused on the intersection of **artificial intelligence**, **circuit design automation**, and **biomedical signal processing**
- Specialized in the co-design of **algorithm** and **hardware** for biomedical signal analysis and human-machine interfaces
- Provided solution to bridge the gap between **cutting-edge AI** algorithms and their practical implementation
- **Principal Investigator** for the FY25 User-Intensive Basic Research (UIBR) project funded by IME, A*STAR
- Achieved the IEEE SSCS Open-Source Ecosystem "Code-a-Chip" **Travel Grant Award**
- Awarded the IEEE CASS **Pre-Doctoral Grant** and IEEE CASS **Student Travel Grant** on IEEE ISCAS 2024
- Achieved the **1st Place** of Respiratory Sound Grand Challenge and **Student Research Grant** on IEEE BioCAS 2023
- Published papers on **TBioCAS**, **DAC**, **ISCAS**, **BioCAS**, **AICAS**, and have submitted recent works to **TCAS-I**

## Education

**Nanyang Technological University (NTU)** *Singapore*

Doctor of Philosophy (Electrical and Electronic Engineering) (EEE) *Jan 2021 - Nov 2024 (Submitted Thesis)*

- **A*STAR Graduate Scholarship (Singapore)**
- **Research Student** at Centre for Integrated Circuits and Systems (CICS/VIRTUS, NTU)
- **Ph.D. Qualifying Examination:** Passed in Aug 2022 with topic: *Time Series Analysis on Edge-AI Hardware for Healthcare Monitoring*
- **Ph.D. Thesis:** Submitted in Nov 2024 with topic: *Software-hardware Co-design for Biomedical Signal Analysis and Human-machine Interface*
- **Key Courses:** Digital IC Design, Digital Communication Systems, Image Analysis and Pattern Recognition, Neural and Fuzzy Systems, Genetic Algorithms and Machine Learning, Robotics and Intelligent Sensors

**Nanyang Technological University (NTU)** *Singapore*

Bachelor of Engineering (Electrical and Electronic Engineering) (EEE) *Aug 2017 - Dec 2020*

- **NTU Science and Engineering Undergraduate Scholarship** (Ministry of Education SM2 Program)
- **Honours (Highest Distinction)** with CGPA: 4.80/5.00
- **Dean's List** (Top 5% of the cohort) for Academic Year (AY) 2018/2019
- **Key Courses:** Intelligent System Design, Computational Intelligence, Artificial Intelligence and Data Mining, Digital Signal Processing (System Design), Digital/Analog Electronics, Computer Communications, Data Structures and Algorithms

**University of California, Los Angeles (UCLA)** *California, United States*

Exchange Program (Electrical and Computer Engineering) (ECE) *Jun 2018 - Jul 2018*

- **Key Courses:** Electrical and Electronic Circuits, Electricity and Magnetism

## Research Experience

**Agile Analog IC Design and Optimization using Multimodal Circuit Representation Learning** *IME*

Analog circuit representation learning, Reinforcement learning *Mar 2025 - Present*

- Develop AI models capable of understanding and predicting circuit behaviours from diverse circuit representations
- Train models to learn design patterns to intelligently modify the circuits to meet design specifications across different technology nodes
- Utilize reinforcement learning for feedback enhancement during inference

**Ultrasound Array Hardware System Design** *IME-NTU*

Beamforming, Ultrasound array optimization *Jun 2024 - Present*

- Proposed a graph neural network to simulate a beamformer array, conducting end-to-end training to optimize array configuration, explore beamforming algorithms, and improve imaging quality
- Utilized circuit-algorithm co-design for an analog/hybrid beamformer to guide circuit design during pre-layout simulations and minimize parasitic effects in post-layout simulations

**Circuit-Algorithm Co-design for Learnable Analog Front-End** *NTU-IME*

Analog front-end, AI-assisted circuit design *Jan 2024 - Aug 2024*

- Proposed a circuit-algorithm co-design framework for learnable audio analog front-end which includes an analog filterbank for feature extraction and a classifier based on neural network
- Designed a holistic framework for achieving superior classification performance and efficient hardware resource utilization
- **Winner of the IEEE SSCS Open-Source Ecosystem "Code-a-Chip" Travel Grant Award**

### Supervised Contrastive Learning Framework and Hardware Implementation on FPGA for Real-time Respiratory Sound Classification

*NTU-IME*

Respiratory sound classification, Supervised contrastive learning, FPGA *Feb 2023 - Jun 2024*

- Proposed a strategy of hybridizing multiple techniques to classify paediatric respiratory sound from the open-source SPRSound database
- Implemented residual neural networks, supervised contrastive learning, mixUp finetuning, and Bayesian optimization to reduce overfitting and enhance classification accuracy
- Performed quantization-aware-training with low hardware expenditure for real-time implementation on Xilinx Zynq ZCU102 PFGA
- **Achieved the 1st place in BioCAS 2023 Grand Challenge**

### Energy Efficient Software-hardware Co-design of Quantized Neural Networks for Continuous Cardiac Monitoring

*NTU-IME*

ECG classification, Neural network quantization, FPGA *Jan 2021 - Aug 2024*

- Proposed dynamically-biased LSTM neural netowrk to achieve faster training convergence and 96.74% ECG classification accuracy when weights are truncated from FP32 to INT4, with only 2.4% accuracy degradation
- Implemented on Xilinx Artix-7 FPGA with 40μW dynamic power consumption
- Proposed quantized recurrent convolutional neural network for ECG signal classification to reduce more than 50% learnable parameters while maintain 98.08% validation accuracy
- Designed pipelining and data reuse within the 1-D convolution kernel on Xilinx Artix-7 FPGA to reduce latency
- Proposed one-hot encoding scheme to convert analog signal to one-dimensional vector
- Simplified the design of ADC and improoved the classification accuracy using quantized LSTM neural network

### Neuromorphic Computing for Keyword Spotting

*NTU-IME*

Spiking-based model, Keyword spotting, MATLAB *Jul 2019 - Dec 2020*

- **NTU Professional Internship (PI)** from *Jul 2019* to *Dec 2019*
- **NTU Final Year Project (FYP)** from *Jan 2020* to *Dec 2020*
- Modelled and simulated leaky integrate-and-fire and Hodgkin-Huxley spiking neurons on MATLAB
- Analysed performance between fast Fourier transform and spike coding on audio signal processing
- Proposed and designed spiking-based neural networks on MATLAB for keyword spotting
- Implemented spiking neurons on MCU to output spike counts with analog input signal

## Achievements

| | |
|---|---|
| Jun 2024 | **IEEE SSCS "Code-a-Chip" Travel Grant Award**, IEEE International Symposium on VLSI Technology & Circuits, *USA* |
| May 2024 | **IEEE CASS Pre-Doctoral Grant**, IEEE International Symposium on Circuits and Systems, *Singapore* |
| May 2024 | **IEEE CASS Student Travel Grant**, IEEE International Symposium on Circuits and Systems, *Singapore* |
| Oct 2023 | **Grand Challenge Award (1st Prize)**, IEEE Biomedical Circuits and Systems Conference, *Canada* |
| Oct 2023 | **Grand Challenge Student Research Grant**, IEEE Biomedical Circuits and Systems Conference, *Canada* |
| Oct 2020 | **A*STAR Graduate Scholarship**, Agency for Science, Technology and Research (A*STAR), *Singapore* |
| Mar 2020 | **Honorable Mention**, Mathematical Contest in Modeling, *Consortium for Mathematics and its Applications, USA* |
| May 2019 | **Champion Team**, Design and Innovation Project Competition, *NTU EEE, Singapore* |
| May 2019 | **Dean's List**, Academic Year 2018/2019, *NTU EEE, Singapore* |
| Jan 2019 | **Successful Participants**, Mathematical Contest in Modeling, *Consortium for Mathematics and its Applications, USA* |
| Jun 2016 | **NTU Science and Engineering Undergraduate Scholarship**, SM2 Program, *NTU & Ministry of Education, Singapore* |

## Technical Skills

| | |
|---|---|
| **Programming** | Python (PyTorch, NumPy, Matplotlib, SciPy, Scikit-learn, Jupyter Notebook) (advanced), MATLAB (advanced), Git (advanced), Verilog (advanced), R (intermediate), C/C++ (intermediate), VHDL (intermediate), JavaScript, SQL |
| **Circuit Design** | Cadence (advanced), Virtuoso (advanced), Ngspice (advanced), LTspice (intermediate), Magic |
| **Writing Skills** | Microsoft Office (Word, PowerPoint, Excel) (advanced), LaTeX (advanced), Markdown (advanced) |
| **Language** | English (proficient), Mandarin (native) |

## Work Experience

### Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR)

*Singapore*

Scientist - Integrated Circuit Design & Systems Department *Jan 2025 - Present*

- Perform system-level beamformer architecture, design, and simulation, to derive circuit-level design specifications
- Beamforming array optimization using AI algorithms
- Design and implementation of beamformer algorithm in hardware
- Work together with team to investigate novel circuit/system solutions to create new inventions

**Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR)** *Singapore*

Research Intern - Integrated Circuit Design & Systems Department *Jul 2019 - Dec 2019*

- Modelled and simulated leaky integrate-and-fire and Hodgkin-Huxley spiking neurons on MATLAB
- Analysed performance between fast Fourier transform and spike coding on audio signal processing
- Proposed spiking-based convolutional neural network for voice keyword recognition
- Participated in weekly team meeting to engage in the state-of-the-art design of analog integrated circuits

# Publications

* Equally Contributed Authors

## Journal Articles

[1] J. Hu, Z. Zhang, C. S. Leow, W. L. Goh, and Y. Gao, "LearnAFE: Circuit-algorithm co-design framework for learnable audio analog front-end," *IEEE Transactions on Circuits and Systems I: Regular Papers*, submitted, 2025.

[2] C. Shen, J. Hu, Y. S. Chong, *et al.*, "A 8.18μW noise-robust keyword spotting chip using spiking-DSCNN and supporting on-device personalization," *IEEE Transactions on Circuits and Systems I: Regular Papers*, to be submitted, 2025.

[3] C. Shen*, J. Hu*, W. L. Goh, Y. S. Chong, A. T. Do, and Y. Gao, "Low-power learnable digital audio feature extractor for always-on keyword spotting in edge devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, submitted, 2025.

[4] Z. Zhang*, J. Hu*, W. L. Goh, and Y. Gao, "A 66.2nW noise-robust acoustic feature extractor featuring bandpass filter with active capacitance multiplier and filterbank learning," *IEEE Transactions on Circuits and Systems I: Regular Papers*, to be submitted, 2025.

[5] J. Hu*, C. S. Leow*, S. Tao, W. L. Goh, and Y. Gao, "Supervised contrastive learning framework and hardware implementation on FPGA for real-time respiratory sound classification," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 19, no. 1, pp. 185–195, 2025. DOI: 10.1109/TBCAS.2024.3409584.

## Conference Proceedings

[1] J. Hu, W. L. Goh, and Y. Gao, "A digital compute-in-memory macro featuring two's complement multiplication for LSTM-based biomedical signal classification," in *58th IEEE International Symposium on Circuits and Systems (ISCAS)*, accepted, 2025.

[2] J. Hu, W. L. Goh, X. Luo, and Y. Gao, "AI-powered agile analog circuit design and optimization," in *AI 4 X Conference 2025*, submitted, 2025.

[3] Z. Cao, J. Hu, W. L. Goh, and Y. Gao, "A 0.58mW dB-linear time gain compensation amplifier with ±0.5-dB gain error for imaging applications," in *58th IEEE International Symposium on Circuits and Systems (ISCAS)*, accepted, 2025.

[4] J. Hu, W. L. Goh, and Y. Gao, "LSTM-based ECG signal classification with multi-level one-hot encoding for wearable applications," in *20th IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2024, pp. 1–5. DOI: 10.1109/BioCAS61083.2024.10798273.

[5] J. Hu, Z. Zhang, C. S. Leow, W. L. Goh, and Y. Gao, "Late breaking results: Circuit-algorithm co-design for learnable audio analog front-end," in *61st ACM/IEEE Design Automation Conference (DAC)*, 2024, pp. 1–2. DOI: 10.1145/3649329.3663496.

[6] S. Tao, J. Hu, W. L. Goh, and Y. Gao, "Convolutional auto-encoder for variable length respiratory sound compression and reconstruction," in *20th IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2024, pp. 1–5. DOI: 10.1109/BioCAS61083.2024.10798320.

[7] S. Tao*, J. Hu*, W. L. Goh, and Y. Gao, "Squeeze-excite fusion based multimodal neural network for sleep stage classification with flexible EEG/ECG signal acquisition circuit," in *57th IEEE International Symposium on Circuits and Systems (ISCAS)*, 2024, pp. 1–5. DOI: 10.1109/ISCAS58744.2024.10557984.

[8] J. Hu, W. L. Goh, and Y. Gao, "Classification of ecg anomaly with dynamically-biased LSTM for continuous cardiac monitoring," in *56th IEEE International Symposium on Circuits and Systems (ISCAS)*, 2023, pp. 1–5. DOI: 10.1109/ISCAS46773.2023.10181690.

[9] J. Hu, C. S. Leow, W. L. Goh, and Y. Gao, "Energy efficient software-hardware co-design of quantized recurrent convolutional neural network for continuous cardiac monitoring," in *5th IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)*, 2023, pp. 1–5. DOI: 10.1109/AICAS57966.2023.10168601.

[10] J. Hu*, C. S. Leow*, S. Tao, W. L. Goh, and Y. Gao, "Supervised contrastive pretrained resnet with mixup to enhance respiratory sound classification on imbalanced and limited dataset," in *19th IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2023, pp. 1–5. DOI: 10.1109/BioCAS58349.2023.10389029.

[11] J. Hu, W. L. Goh, and Y. Gao, "Dynamically-biased fixed-point LSTM for time series processing in AIoT edge device," in *3rd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)*, 2021, pp. 1–4. DOI: 10.1109/AICAS51828.2021.9458508.

[12] J. Hu, W. L. Goh, Z. Zhang, and Y. Gao, "Voice keyword recognition based on spiking convolutional neural network for human-machine interface," in *3rd IEEE International Conference on Intelligent Autonomous Systems (ICoIAS)*, 2020, pp. 77–82. DOI: 10.1109/ICoIAS49312.2020.9081859.

# Volunteer and Leadership

**IEEE Singapore Student Branch & Circuits and Systems Society** *Singapore*

IEEE CASS Student Branch Chapter Chair of NTU *Nov 2023 - Dec 2024*

- Organized workshops together with IEEE CASS Singapore chapter

**NTU Hall of Residence 3 Residential Education** *Singapore*

Student Organizer of Edible Gardens *Aug 2018 - Dec 2019*

- Reclaimed planting areas near Hall of Residence 3
- Organized and planted vegetables, herbs and spices in planter boxes

**NTU EEE Design and Innovation Project (DIP)** *Singapore*

Group Leader *Jan 2019 - May 2019*

- Organized weekly meeting and distributed work to develop graph convolutional neural network to predict the transmission direction of dengue fever within Singapore
- **Achieved the 1st place in DIP competition**

**NTU Hall of Residence 3 (with SM2 Program)** *Singapore*

Leader of 20th Batch & Buddy of 21st Batch *Aug 2016 - May 2018*

- Organized monthly events with hall mentors to celebrate residents' birthdays and multicultural festivals
- Assisted 21st batch students in settling into life at NTU and Singapore

**Chingay 2018** *Singapore*

Performer *Aug 2017 - Mar 2018*

- Attended regular training and rehearsals
- Participated in a two-day showcase @ Marina Bay for an audience of 20,000

**Red Cross Youth NTU Chapter** *Singapore*

Organization Volunteer *Aug 2017 - Dec 2017*

- Collaborated with the Red Cross and a team of volunteers to plan and coordinate Blood Donation Drive 2017
- Successfully executed a blood donation event from 24th - 27th October in NTU

**References available upon request.**